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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/538,469	03/29/2000	Kouki Ogawa	Q58486	6688
7:	590 01/21/2003			
Sughrue Mion Zinn MacPeak & Seas PLLC 2100 Pennsylvania Avenue NW			EXAMINER	
			HA, NATHAN W	
Washington, D	C 20037		<u> </u>	
			ART UNIT	PAPER NUMBER
		•	2814	
			DATE MAILED: 01/21/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

•	Application No.	Applicant(s)	
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Office Action Summons	09/538,469	OGAWA ET AL.	$\mathcal{M}$
Office Action Summary	Examiner	Art Unit	
The MAILING DATE of this communication ap	Nathan W. Ha	2814	PSS
The MAILING DATE of this communication ap Period for Reply	pears on the cover sheet with	tii correspondence addi	
A SHORTENED STATUTORY PERIOD FOR REPL THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1. after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a recommunication of the period for reply is specified above, the maximum statutory period.  - Failure to reply within the set or extended period for reply will, by statu.  - Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).  Status	136(a). In no event, however, may a repoly within the statutory minimum of thirty will apply and will expire SIX (6) MONTI the cause the application to become ABA	ly be timely filed  (30) days will be considered timely.  HS from the mailing date of this com.  NDONED (35 U.S.C. § 133).	munication.
1)⊠ Responsive to communication(s) filed on <u>20</u>	November 2002 .	-	
2a)  This action is <b>FINAL</b> . 2b)⊠ T	his action is non-final.		
Since this application is in condition for allov closed in accordance with the practice unde Disposition of Claims	vance except for formal matte r <i>Ex parte Quayle</i> , 1935 C.D	ers, prosecution as to the .11, 453 O.G. 213.	merits is
4)⊠ Claim(s) <u>1-13 and 16-18</u> is/are pending in th			
4a) Of the above claim(s) is/are withdra	awn from consideration.		
5) Claim(s) is/are allowed.			
6)⊠ Claim(s) <u>1-13 and 16-18</u> is/are rejected.			
7) Claim(s) is/are objected to.			
8) Claim(s) are subject to restriction and	or election requirement.		
Application Papers		v	
9) The specification is objected to by the Examir		. F	
10) ☐ The drawing(s) filed on is/are: a) ☐ acc			
Applicant may not request that any objection to	he drawing(s) be neid in abeyar	sannroyed by the Evaminer	
11) The proposed drawing correction filed on  If approved, corrected drawings are required in r		sapproved by the Examinor	•
12) The oath or declaration is objected to by the E			
Priority under 35 U.S.C. §§ 119 and 120			
13) Acknowledgment is made of a claim for foreign	an priority under 35 U.S.C. &	119(a)-(d) or (f)	
a) ☐ All b) ☐ Some * c) ☐ None of:	gri priority under 00 0.0.0. 3	110(4) (4) 51 (1).	
· · · · · · · · · · · · · · · · · · ·	nts have been received		
		inlication No	
			tage
<ul> <li>3. Copies of the certified copies of the principle.</li> <li>application from the International E</li> <li>* See the attached detailed Office action for a list</li> </ul>	Bureau (PCT Rule 17.2(a)).		
14) Acknowledgment is made of a claim for domes	stic priority under 35 U.S.C. §	119(e) (to a provisional a	application).
a) The translation of the foreign language p	rovisional application has be	en received.	
Attachment(s)			
<ol> <li>Notice of References Cited (PTO-892)</li> <li>Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>Information Disclosure Statement(s) (PTO-1449) Paper No(s)</li> </ol>	5) Notice of Ir	ummary (PTO-413) Paper No(s formal Patent Application (PTO	

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### **DETAILED ACTION**

## Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
- 3. Claims 1-13 and 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Zavrel, Jr. et al. (US. 6,218,729 B1, hereinafter, Zavrel, previously cited.)

In regard to claims 1-2, 4, 9-10, in figs. 3 and 8-9, Zavrel discloses a printed wiring substrate 822 having a planar surface and a built-in capacitor 804 on which an IC chip 820 is mounted, the printed substrate comprising a capacitor cavity selected from the group consisting of a closed-bottom cavity 850 and a through hole cavity 856, see fig. 8. The capacitor comprises

a pair of electrodes 860, 862; and

a plurality of capacitor terminals 810, 812 projecting beyond the surface of the printed substrate, wherein the respective capacitor terminals are electrically connected to one or the other paired electrodes, figs. 8-9;

the printed wiring substrate 822 comprises a plurality of substrate terminals, for example, 844, 840;

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the IC chip 820 comprises a plurality of connection-to-capacitor terminals 828 and plurality of connection-to-substrate terminals, also labeled as 828, on the right side of fig. 8;

the plurality of capacitor terminals of the capacitor are respectively flip-chipbonded to a plurality of connection-to-capacitor terminals of the IC chip, see fig. 8; and

the plurality of the substrate terminals of the printed wiring substrate are respectively flip-chip-bonded to a plurality of connection-to-substrate terminals of the IC chip. The region directly below the die where the capacitor formed is considered as a cavity therein. This capacitor, clearly, is constructed in an accommodating cavity embedded in the substrate, see fig. 8.

In regard to claim 3, the IC-chip-carrying printed wiring substrate is a CSP adapted for mounting an IC chip, see col. 2, first paragraph, and fig. 8.

In regard to claim 5, see col. 3, first paragraph, see also fig. 8.

In regard to claim 6, see above discussion of claim 1; further see fig. 8, the plurality of capacitor terminals and the plurality of substrate terminals are substantially coplanar.

In regard to claims 7-8, see fig. 9.

In regard to claims 11-12, see fig. 9.

In regard to claim 13, in fig. 8, the balls 830 are used for connecting to another circuit substrate, inherently.

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In regard to claims 16-18, Zavrel further discloses the printed wiring substrate comprises a core substrate made of resin and a capacitor accommodation cavity for the capacitor; and

the capacitor comprises a dielectric layer made of ceramic and electrodes arranged in alternative layers, see figs. 3 and 8 and col. 5, lines 30-45, and the abstract.

## Response to Arguments

4. Applicant's arguments filed 3/18/02 have been fully considered but they are not persuasive. For instance, Applicants contend that Zavrel et al., '729, does not disclose a cavity that formed by vias. According to fig. 8 and discussions above, Zavrel et al. in fact discloses a accommodation cavity defined by vias 850, 856, and the bottom layer 812; this cavity is formed for the same purpose as claimed in the instant application, containing a capacitor in the substrate. Therefore, the cavity is inherently defined therein.

#### Conclusion

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and 308-3432 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Nathan Ha January 14, 2003

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